128K X 36, 256K X 18
3.3V Synchronous SRAMs
3.3V I/O, Flow-Through Outputs
Burst Counter, Single Cycle Deselect

IDT71V3577S
IDT71V3579S
IDT71V3577SA
IDT71V3579SA

Features

- **128K x 36, 256K x 18 memory configurations**
- **Supports fast access times:**
  Commercial:
  – *7.5ns up to 117MHz clock frequency*
  Commercial and Industrial:
  – *8.0ns up to 100MHz clock frequency*
  – *8.5ns up to 87MHz clock frequency*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **3.3V I/O**
- **Optional - Boundary Scan JTAG Interface (IEEE 1149.1 compliant)**
- **Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array**

Description

The IDT71V3577/79 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V3577/79 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V3577/79 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V3577/79 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A_0-A_{17}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
TMS	Test Mode Select	Input	Synchronous
TDI	Test Data Input	Input	Synchronous
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	Synchronous
$\overline{TRST}$	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

NOTE:
1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V3579.

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Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial Values	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature Supply Voltage

Grade	Temperature(1)	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5280 tbl 04

NOTES:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.8	V

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NOTES:
1. V_{IH} (max) = VDDQ + 1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100 Pin TQFP Capacitance
(T_A = +25° C, f = 1.0mhz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

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119 BGA Capacitance
(T_A = +25° C, f = 1.0mhz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

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165 fBGA Capacitance
(T_A = +25° C, f = 1.0mhz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

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NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	ZZ , $\overline{LBO}$ and JTAG Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

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NOTE:
1. The $\overline{LBO}$, TMS, TDI, TCK and $\overline{TRST}$ pins will be internally pulled to V_{DD} and the ZZ in will be internally pulled to V_{SS} if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (1)

Symbol	Parameter	Test Conditions	7.5ns	8ns		8.5ns		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	255	200	210	180	190	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	30	30	35	30	35	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX} (2,.3)	90	85	95	80	90	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	30	30	35	30	35	mA

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NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 3.3V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

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AC Test Load

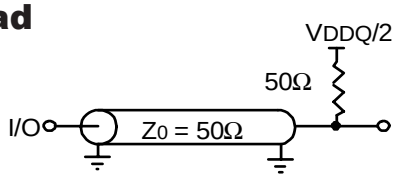

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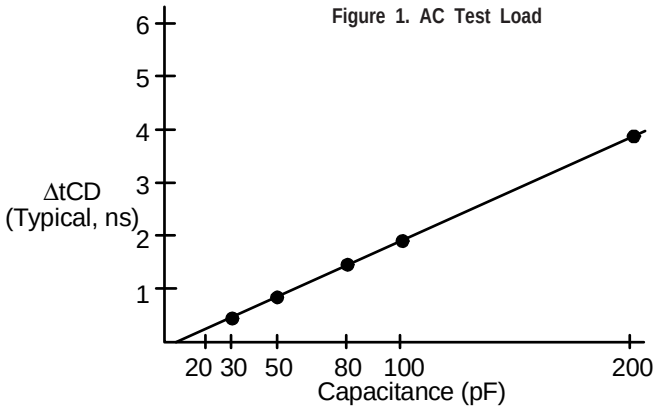
Figure 1. AC Test Load



5280 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

AC Electrical Characteristics

(VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	7.5ns[5]		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameter								
t_{CYC}	Clock Cycle Time	8.5	—	10	—	11.5	—	ns
t_{CH}[1]	Clock High Pulse Width	3	—	4	—	4.5	—	ns
t_{CL}[1]	Clock Low Pulse Width	3	—	4	—	4.5	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	2	—	ns
t_{CLZ}[2]	Clock High to Output Active	0	—	0	—	0	—	ns
t_{CHZ}[2]	Clock High to Data High-Z	2	3.5	2	3.5	2	3.5	ns
t_{OE}	Output Enable Access Time	—	3.5	—	3.5	—	3.5	ns
t_{OLZ}[2]	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Enable High to Output High-Z	—	3.5	—	3.5	—	3.5	ns
Set Up Times								
t_{SA}	Address Setup Time	1.5	—	2	—	2	—	ns
t_{SS}	Address Status Setup Time	1.5	—	2	—	2	—	ns
t_{SD}	Data In Setup Time	1.5	—	2	—	2	—	ns
t_{SW}	Write Setup Time	1.5	—	2	—	2	—	ns
t_{SAV}	Address Advance Setup Time	1.5	—	2	—	2	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	2	—	2	—	ns
Hold Times								
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t_{ZZR}[3]	ZZ Recovery Time	100	—	100	—	100	—	ns
t_{CFG}[4]	Configuration Set-up Time	34	—	40	—	50	—	ns

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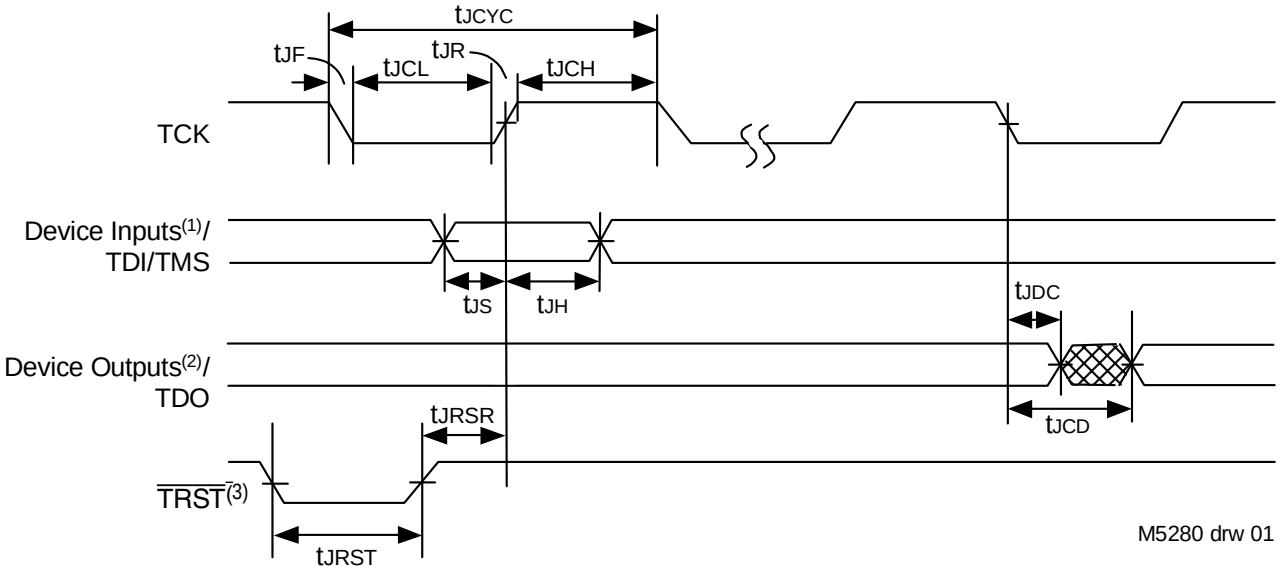
NOTES:

1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.
5. Commercial temperature range only.

JTAG Interface Specification (SA Version only)



NOTES:
1. Device inputs = All device inputs except TDI, TMS and $\overline{\text{TRST}}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{\text{TRST}}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{\text{TRST}}$ is an optional JTAG reset.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5(1)	ns
t_{JF}	JTAG Clock Fall Time	—	5(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

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NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

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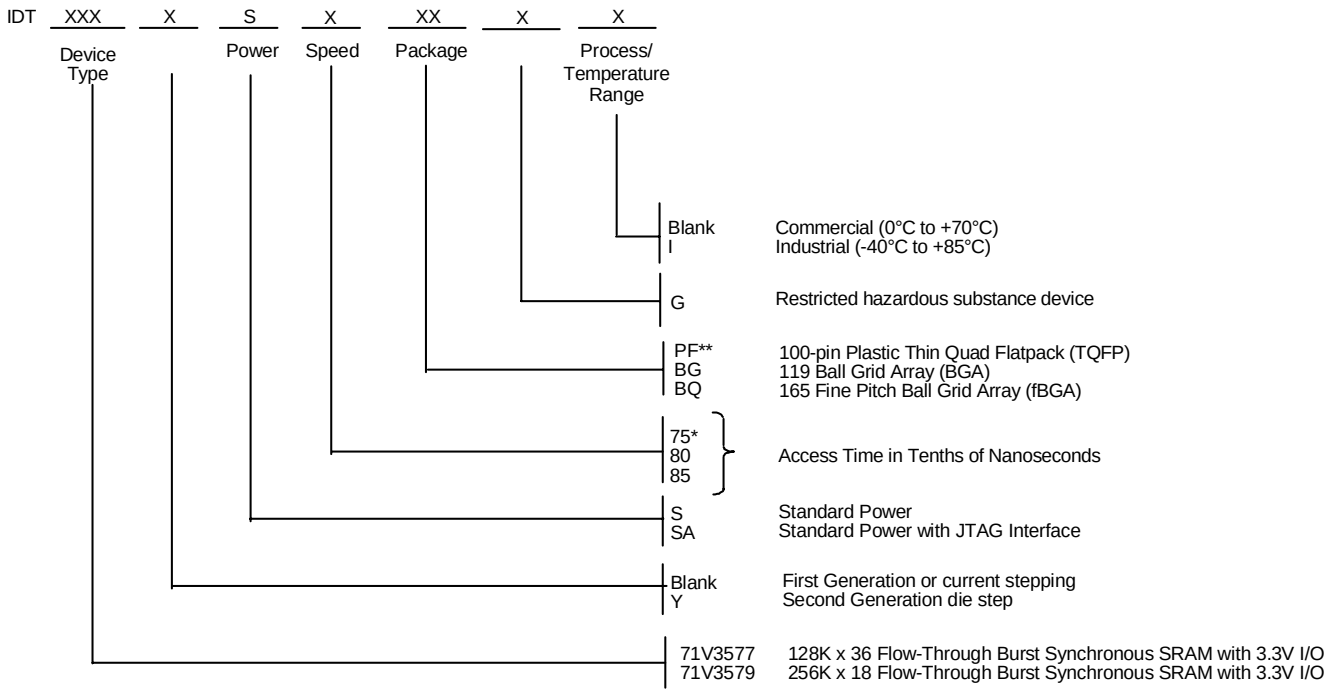
NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

Ordering Information



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*Commercial temperature range only.
** JTAG (SA version) is not available with 100 pin TQFP package

Package Information

100-Pin Thin Quad Plastic Flatpack (TQFP)
119 Ball Grid Array (BGA)
165 Fine Pitch Ball Grid Array (fBGA)
Information available on the IDT website